OCTAL ±100V 2A 3-LEVEL ULTRASOUND PULSER

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Rev.2.0_01

The ABLIC Inc. HDL6M05584 is an octal, 3-level RTZ, high-voltage, high-speed ultrasound pulser.
The HDL6M05584 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Octal 3-level pulser with active T/R switch with 2-input per channel

Features

- 0 to ±100V output voltage
- ±2A source and sink peak current for pulsing (V_{PP}/V_{NN})
- ±1A source and sink peak current for active ground clamp
- 250Ω (±0.1A) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 15Ω active T/R switch with 2-bit turn-on timing control
- 20MHz output frequency @±60V output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 4-mode output current control
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead 9x9mm QFN package (RoHS compliant)

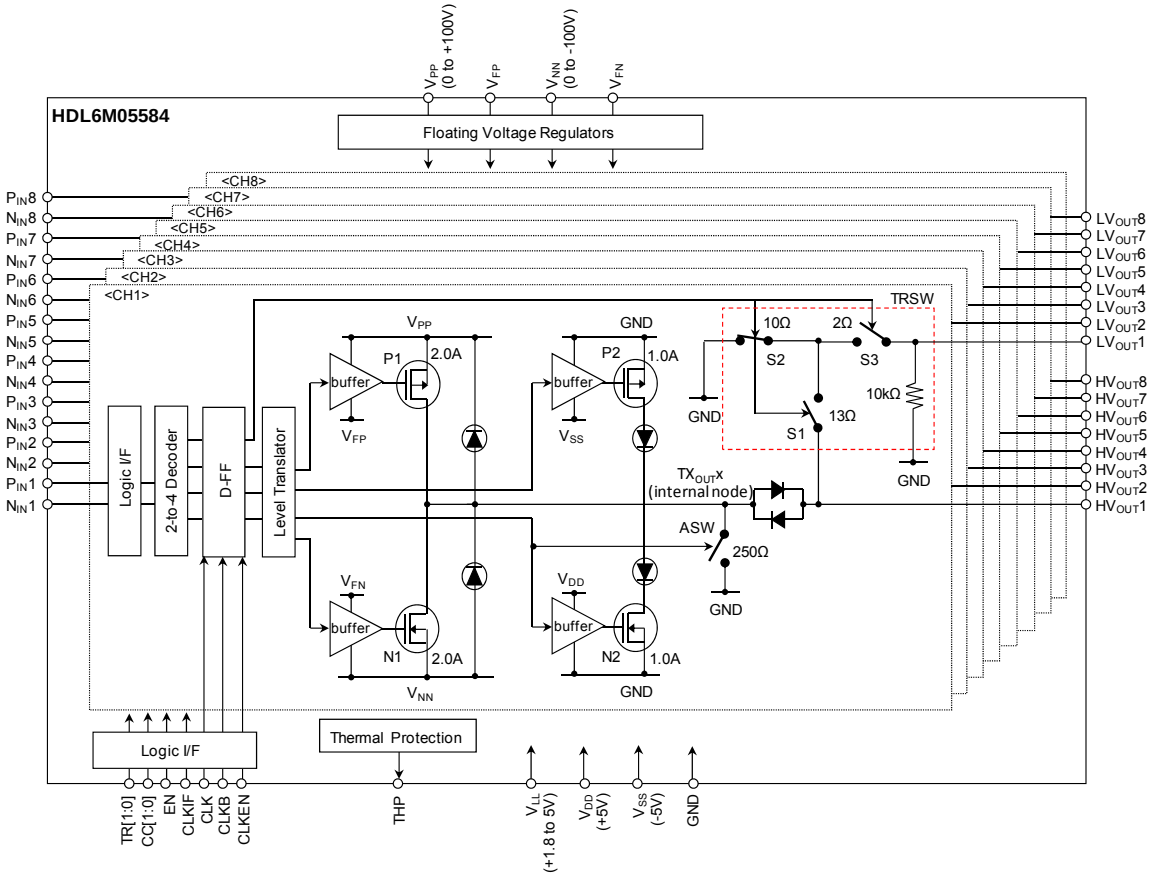


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Negative supply voltage	V_{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V_{PP}	-0.5 to +105	V	
5	Negative high-voltage supplies	V_{NN}	-105 to +0.5	V	
6	High-voltage outputs (x=1~8)	$HV_{OUT}x$	-105 to +105	V	
7	Low-voltage outputs (x=1~8)	$LV_{OUT}x$	-1 to +1	V	
8	THP (Thermal Protection) output	THP	-0.4 to +7	V	
9	All Logic input voltages (x=1~8)	$P_{IN}x$, $N_{IN}x$, EN, CLKEN, CLK, CLKB, CLKIF, CC[1:0], TR[1:0]	-0.4 to +7	V	
10	Operating junction temperature	T_{Jop}	-20 to +150	°C	
11	Operating free-air Temperature	T_A	0 to +75	°C	
12	Storage temperature	T_{STG}	-55 to +150	°C	
13	Maximum power dissipation	P_{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V_{PP}	0	-	100	V	
5	Negative high-voltage supplies	V_{NN}	-100	-	0	V	
6	IC substrate voltage *	V_{SUB}	-	0	-	V	
7	V_{PP}, V_{NN} slew rate	SR_{MAX}	-	-	25	V/ms	

NOTE: * The package exposed pad internally connected to the chip substrate must be soldered to the ground.

2.2 Logic Inputs

Clock (CLK) mode synchronizes data inputs $P_{IN}x$, $N_{IN}x$ (x=1~8) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. $P_{IN}x$ and $N_{IN}x$ are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. Connect 100Ω between CLK and CLKB. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. $P_{IN}x$ and $N_{IN}x$ are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition	
1	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V		
2	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V		
3	Logic input capacitance	C_{IN}	-	3	-	pF		
4	Logic input high current *1	I_{IH}	-10	-	10	μA		
5	Logic input low current *2	I_{IL}	-10	-	10	μA		
6	Input rise/fall time	t_r, t_f	-	-	800	ps	CLK≥100MHz	CMOS CLK mode 10~90% CLK, CLKB, $P_{IN}x$, $N_{IN}x$
			-	-	2.0	ns	CLK<100MHz	
7	Input clock frequency	f_{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.3	
8	Duty cycle	D_{CLK}	40	50	60	%		
9	Data Setup time	t_{SU}	1.4	-	-	ns	CLK mode, $P_{IN}x$, $N_{IN}x$ to CLK/CLKB See Fig.3	
10	Data Hold time	t_{HLD}	1.4	-	-	ns		

NOTE:

*1) TR[1:0] have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

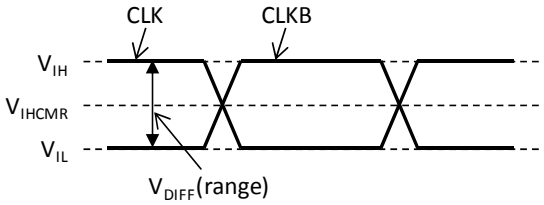
*2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	-	-	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	|CLK-CLKB| differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	
7	High-level input current	I_{IH}	-	-	5.8	mA	
8	Low-level input current	I_{IL}	-	-	5.8	mA	
9	Input rise/fall time	t_r, t_f	-	-	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.3
11	Duty cycle	D_{CLK}	40	50	60	%	

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range (V_{DIFF}(range))



Differential input voltage peak to peak swing (V_{DIFF}(p-p))

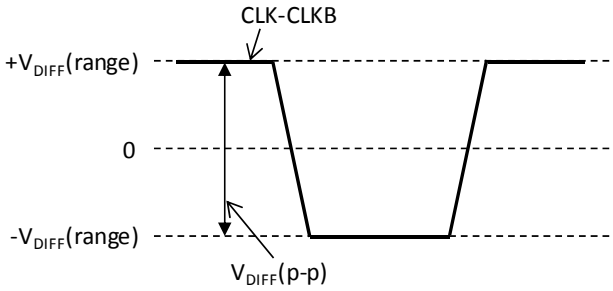
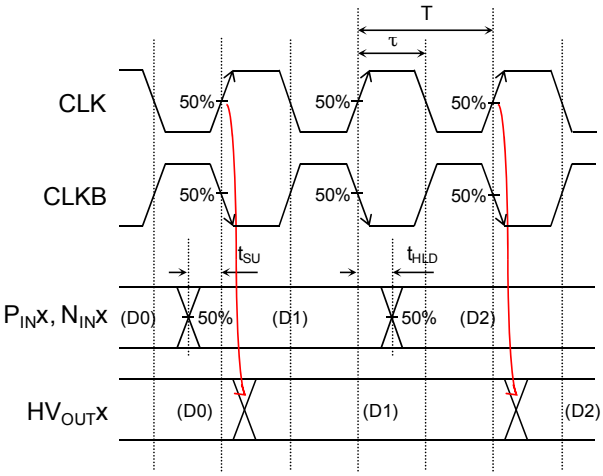


Fig.2 LVDS clock inputs

LVDS/CMOS CLK mode (CLKEN=0)



TP mode (CLKEN=1)

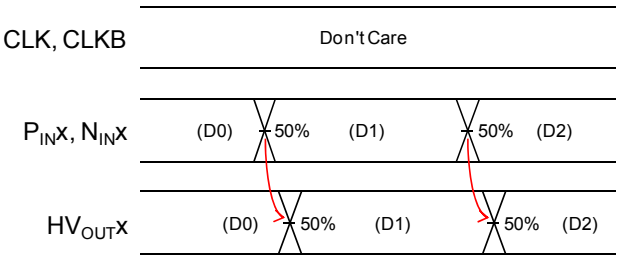


Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

3. Typical Application Circuit

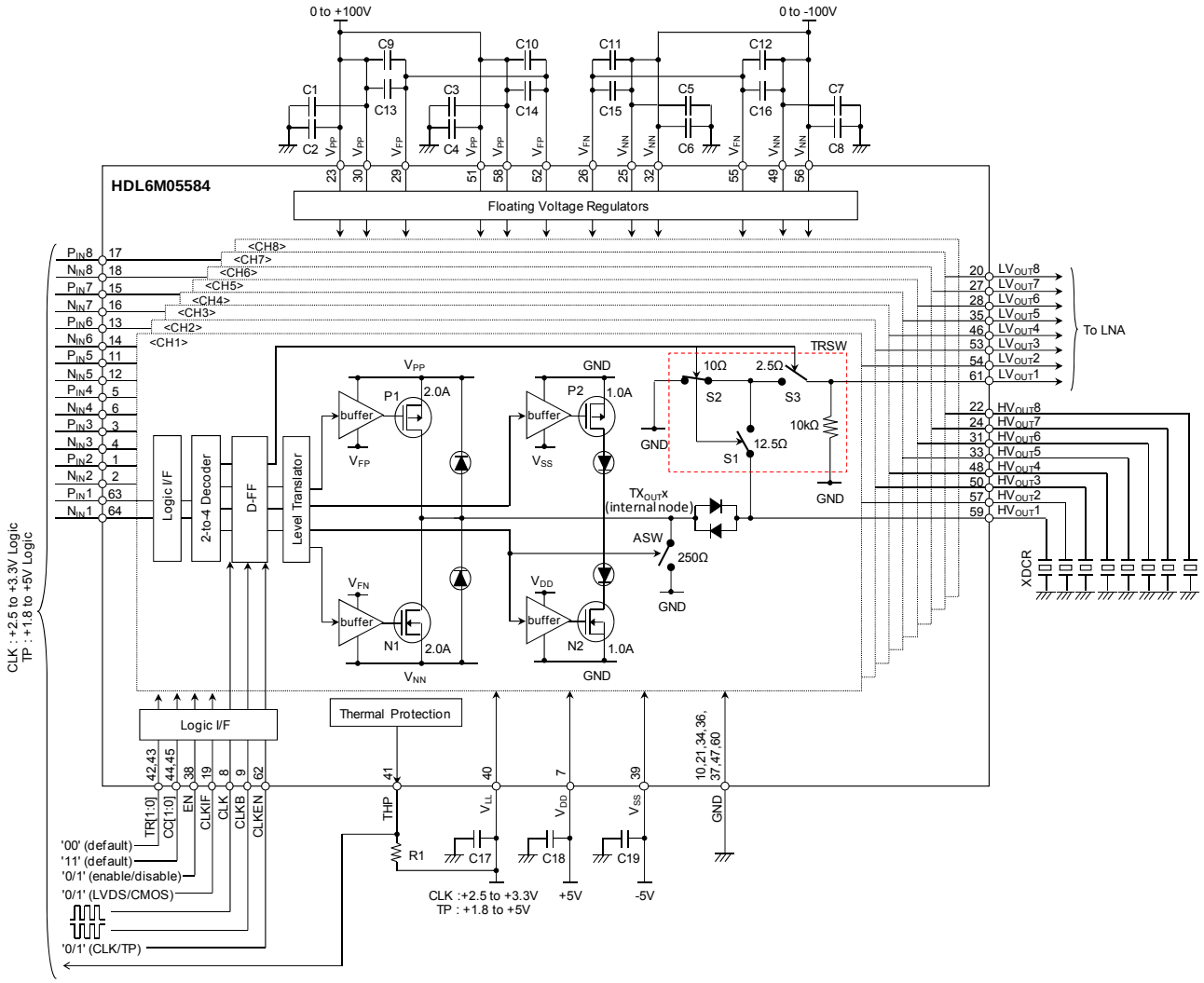


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, V_{PP}/V_{NN}, can draw fast transient currents up to ±2.0A. Therefore, ceramic capacitors of ≥200V 0.1μF to 1μF (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 10μF (C9~12), ≥16V 100nF (C13~16), and ≥16V 0.1μF to 1μF (C17~19) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{FP}/V_{FN}, and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. Please refer to Mode Control Tables for detailed CC[1:0] and TR[1:0] setting.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, CLK=CLKB=100MHz/0(CLKEN=0/1), TR[1:0]='00',
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP	I_{LLQD}	-	0.03	-	mA	Quiescent current-1 EN=1(Disable) $P_{IN}x=N_{IN}x=0$ Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=+/-100V
		LVDS CLK		-	0.08	-	mA	
		CMOS CLK		-	0.13	-	mA	
2	V_{DD} current	TP	I_{DDQD}	-	2.8	-	mA	
		LVDS CLK		-	2.8	-	mA	
		CMOS CLK		-	2.8	-	mA	
3	V_{SS} current		I_{SSQD}	-	0.63	-	mA	
4	V_{PP} current		I_{PPQD}	-	0.03	-	mA	
5	V_{NN} current		I_{NNQD}	-	0.04	-	mA	
6	V_{LL} current	TP	I_{LLQE}	-	0.08	-	mA	Quiescent current-2 EN=0(Enable) $P_{IN}x=N_{IN}x=0$ Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=+/-100V
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
7	V_{DD} current	TP	I_{DDQE}	-	10	-	mA	
		LVDS CLK		-	30	-	mA	
		CMOS CLK		-	28	-	mA	
8	V_{SS} current		I_{SSQE}	-	9.3	-	mA	
9	V_{PP} current		I_{PPQE}	-	0.15	-	mA	
10	V_{NN} current		I_{NNQE}	-	0.15	-	mA	
11	V_{LL} current	TP	I_{LLPW}	-	0.08	-	mA	PW operating current EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level 2-cycle f=5MHz, PRT=200µs V_{PP}/V_{NN}=+/-60V
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
12	V_{DD} current	TP	I_{DDPW}	-	10	-	mA	
		LVDS CLK		-	34	-	mA	
		CMOS CLK		-	32	-	mA	
13	V_{SS} current		I_{SSPW}	-	9.3	-	mA	
14	V_{PP} current		I_{PPPW}	-	4.2	-	mA	
15	V_{NN} current		I_{NNPW}	-	4.9	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
16	V_{LL} current	TP	I_{LLCW3}	-	0.43	-	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
		LVDS CLK		-	0.53	-	mA	
		CMOS CLK		-	0.48	-	mA	
17	V_{DD} current	TP	I_{DDCW3}	-	42	-	mA	
		LVDS CLK		-	64	-	mA	
		CMOS CLK		-	61	-	mA	
18	V_{SS} current		I_{SSCW3}	-	27	-	mA	
19	V_{PP} current		I_{PPCW3}	-	217	-	mA	
20	V_{NN} current		I_{NNCW3}	-	220	-	mA	
21	V_{LL} current	TP	I_{LLCW2}	-	0.48	-	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
22	V_{DD} current	TP	I_{DDCW2}	-	38	-	mA	
		LVDS CLK		-	60	-	mA	
		CMOS CLK		-	57	-	mA	
23	V_{SS} current		I_{SSCW2}	-	23	-	mA	
24	V_{PP} current		I_{PPCW2}	-	208	-	mA	
25	V_{NN} current		I_{NNCW2}	-	211	-	mA	
26	V_{LL} current	TP	I_{LLCW1}	-	0.48	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
27	V_{DD} current	TP	I_{DDCW1}	-	34	-	mA	
		LVDS CLK		-	56	-	mA	
		CMOS CLK		-	53	-	mA	
28	V_{SS} current		I_{SSCW1}	-	18	-	mA	
29	V_{PP} current		I_{PPCW1}	-	195	-	mA	
30	V_{NN} current		I_{NNCW1}	-	198	-	mA	
31	V_{LL} current	TP	I_{LLCW0}	-	0.53	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
		LVDS CLK		-	0.63	-	mA	
		CMOS CLK		-	0.58	-	mA	
32	V_{DD} current	TP	I_{DDCW0}	-	28	-	mA	
		LVDS CLK		-	49	-	mA	
		CMOS CLK		-	47	-	mA	
33	V_{SS} current		I_{SSCW0}	-	13	-	mA	
34	V_{PP} current		I_{PPCW0}	-	169	-	mA	
35	V_{NN} current		I_{NNCW0}	-	173	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	$HV_{OUT}x$ output voltage range	$HV_{OUT}x$	-100	-	+100	V	
2	$HV_{OUT}x$ high-side peak current	I_{OH}	-	2.0	-	A	V_{PP}/V_{NN}=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	V_{PP}/V_{NN}=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	V_{PP}/V_{NN}=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	V_{PP}/V_{NN}=+/-60V Current mode 0 (CC[1:0]='00')
3	$HV_{OUT}x$ high-side GND clamp peak current	I_{OHCL}	-	1.0	-	A	V_{PP}/V_{NN}=+/-60V
4	$HV_{OUT}x$ low-side peak current	I_{OL}	-	2.0	-	A	V_{PP}/V_{NN}=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	V_{PP}/V_{NN}=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	V_{PP}/V_{NN}=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	V_{PP}/V_{NN}=+/-60V Current mode 0 (CC[1:0]='00')
5	$HV_{OUT}x$ low-side GND clamp peak current	I_{OLCL}	-	1.0	-	A	V_{PP}/V_{NN}=+/-60V
6	$HV_{OUT}x$ high-side on-resistance	R_{ONH}	-	10	-	Ω	I_{OH}=100mA Current mode 3 (CC[1:0]='11')
			-	13	-	Ω	I_{OH}=100mA Current mode 2 (CC[1:0]='10')
			-	18	-	Ω	I_{OH}=100mA Current mode 1 (CC[1:0]='01')
			-	31	-	Ω	I_{OH}=100mA Current mode 0 (CC[1:0]='00')
7	$HV_{OUT}x$ high-side GND clamp on-resistance	R_{ONHCL}	-	21	-	Ω	I_{OHCL}=100mA
8	$HV_{OUT}x$ low-side on-resistance	R_{ONL}	-	9	-	Ω	I_{OL}=100mA Current mode 3 (CC[1:0]='11')
			-	12	-	Ω	I_{OL}=100mA Current mode 2 (CC[1:0]='10')
			-	17	-	Ω	I_{OL}=100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	I_{OL}=100mA Current mode 0 (CC[1:0]='00')
9	$HV_{OUT}x$ low-side GND clamp on-resistance	R_{ONLCL}	-	20	-	Ω	I_{OLCL}=100mA
10	$HV_{OUT}x$ off-capacitance	C_{HVOFF}	-	20	-	pF	$TX_{OUT}x$=GND, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25°C, TR[1:0]='00', CC[1:0]='11', CLK=CLKB=100MHz/0(CLKEN=0/1), HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	Output frequency		f_{OUT}	-	20	-	MHz		
2	Output rise propagation delay	TP mode	t_{dr}	-	31	-	ns	See Fig.5	
		CLK mode		-	37	-	ns		
3	Output fall propagation delay	TP mode	t_{df}	-	31	-	ns		
		CLK mode		-	37	-	ns		
4	Output rise propagation delay clamp	TP mode	t_{drCL}	-	31	-	ns		
		CLK mode		-	37	-	ns		
5	Output fall propagation delay clamp	TP mode	t_{dfCL}	-	31	-	ns		
		CLK mode		-	37	-	ns		
6	Propagation delay matching		Δt_d	-	±1	±3	ns		
7	Output rise time		t_r	-	16	-	ns	CC[1:0]='11'	See Fig.5
				-	24	-	ns	CC[1:0]='10'	
				-	34	-	ns	CC[1:0]='01'	
				-	44	-	ns	CC[1:0]='00'	
			t_{rCL}	-	25	-	ns		
8	Output fall time		t_f	-	16	-	ns	CC[1:0]='11'	
				-	24	-	ns	CC[1:0]='10'	
				-	34	-	ns	CC[1:0]='01'	
				-	44	-	ns	CC[1:0]='00'	
			t_{fCL}	-	25	-	ns		
9	2nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f_{OUT}=5MHz See Fig.6	
10	Pulse cancellation		HDPC	-	-40	-	dBc		
			HDPC2	-	-40	-	dBc		
11	RMS output jitter		t_J	-	10	-	ps	Bipolar CW, f_{OUT}=5MHz V_{PP}/V_{NN}=+/-5V	
12	Crosstalk between channels		X_{TLK}	-	-70	-	dB	f_{OUT}=5MHz, $10V_{p-p}$, HV_{OUT} load=50Ω	
13	Output enable time	TP	t_{EN}	-	31	-	ns	See Fig.7	
		LVDS CLK		-	120	-	ns		
		CMOS CLK		-	140	-	ns		
14	Output disable time		t_{DS}	-	37	-	ns		
15	Clock mode enable time		t_{CLKEN}	-	37	-	ns		
16	Clock mode disable time		t_{CLKDS}	-	37	-	ns		

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, T_A=25°C, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	$LV_{OUT}x$ output voltage range		$LV_{OUT}x$	-0.85	-	+0.85	V	
2	TRSW on-resistance		R_{ONTR}	-	15	-	Ω	$HV_{OUT}x$=100mV, $LV_{OUT}x$=0V
3	TRSW on-capacitance		C_{ONTR}	-	12	-	pF	$LV_{OUT}x$=0V
4	TRSW off-resistance on HVOUTx		$R_{OFFTRHV}$	1	-	-	MΩ	
5	TRSW off-resistance on LVOUTx		$R_{OFFTRLV}$	8	10	12	kΩ	
6	Spike voltage on $HV_{OUT}x$ and $LV_{OUT}x$		V_{TRN}	-	-	50	mV_{PP}	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $LV_{OUT}x$
7	TRSW turn-on time	TR[1:0]='00'	t_{dTRON}	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.8
		TR[1:0]='01'		-	400	-	ns	
		TR[1:0]='10'		-	500	-	ns	
		TR[1:0]='11'		-	600	-	ns	
8	TRSW turn-off time		t_{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time		t_{TXSU}	100	-	-	ns	$P_{IN}x=N_{IN}x$=0 (GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R_{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FHVD}	-	1.0	-	V	I_F=100mA
			-	1.2	-	V	I_F=200mA
2	Reverse voltage	V_{RHVD}	200	-	-	V	I_R=1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FLVD}	-	1.1	-	V	I_F=100mA
			-	1.25	-	V	I_F=200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=2.5V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

5. Switching Time Diagram

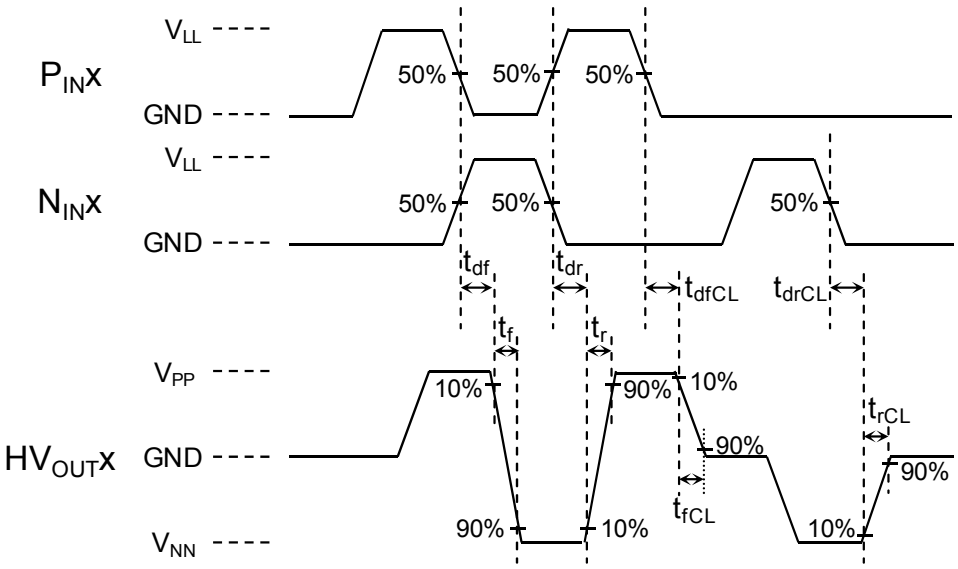
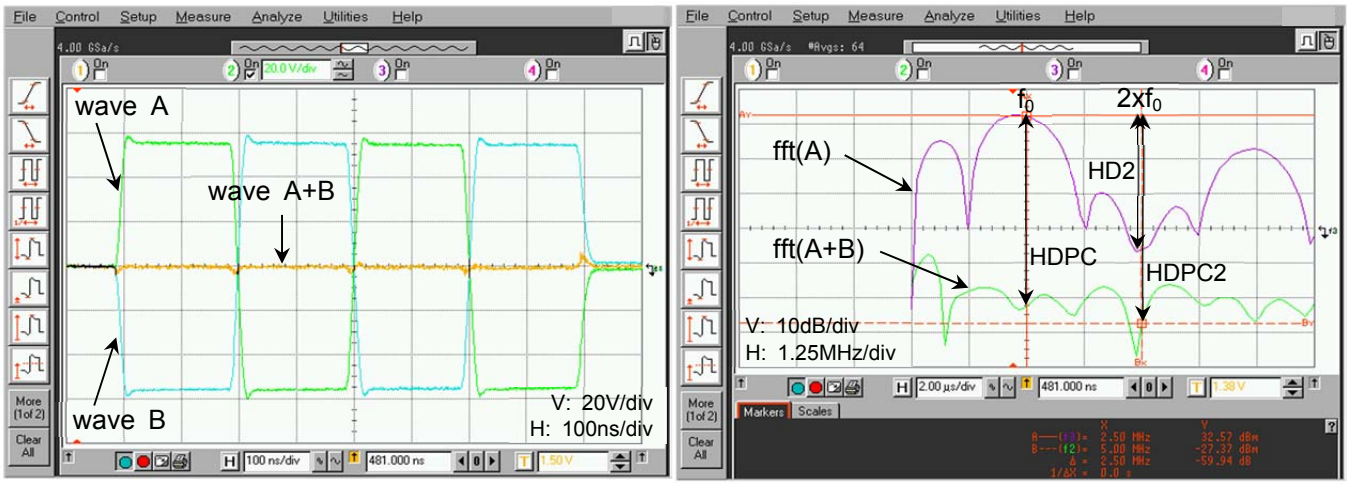


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: VPP/VNN=+/-60V, f_0=2.5MHz, 2-cycle, HV_{OUT} load=220pF//200Ω

Fig.6 2nd harmonic distortion and Pulse cancellation

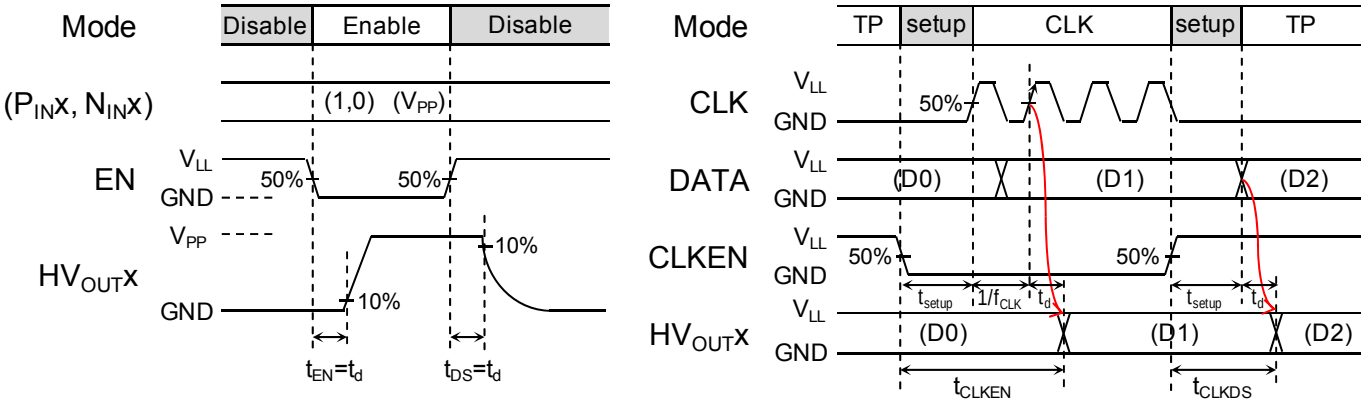


Fig.7 Output enable/disable and Clock enable/disable time

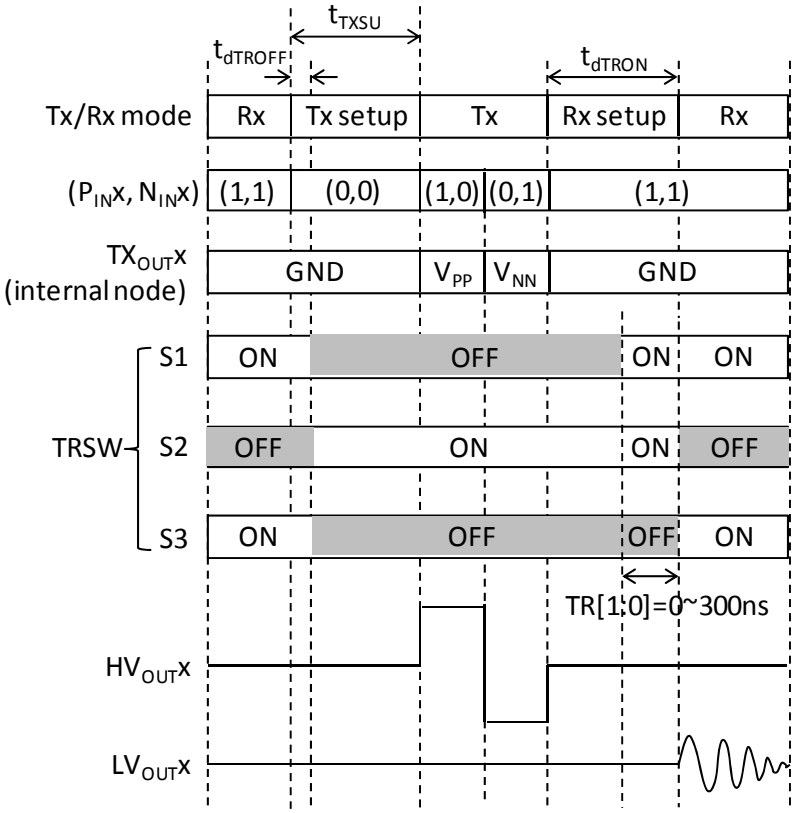


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control tables

Table 13 Truth table

Logic Inputs			Internal MOSFET state								Output state	
EN	**P_{IN}x**	**N_{IN}x**	**P1**	**N1**	**P2**	**N2**	**ASW**	**TRSW**			**TX_{OUT}x**	**LV_{OUT}x**
			+HV	-HV	GND	GND	GND	S1	S2	S3	(internal node)	
0	0	0	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	0	1	OFF	**ON**	OFF	OFF	OFF	OFF	**ON**	OFF	-HV	10kΩ
0	1	0	**ON**	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV	10kΩ
0	1	1	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	HV_{OUT}x
1	X	X	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	HiZ	10kΩ

Note: V_{PP}/ V_{NN}=+/-HV, x=1~8

Table 14 P1/N1 drive current mode

			Iout [A]	
Current Mode	CC1	CC0	P1	N1
0	0	0	0.5	0.5
1	0	1	1	1
2	1	0	1.5	1.5
3	1	1	2	2

Note:
Recommended mode is as follows:

- Current mode 2 or 3 for high amplitude short cycle pulse waveforms, or for driving heavy load
- Current mode 0 or 1 for low amplitude long pulse train waveforms (e.g. CW), or for driving light load

Table 15 TRSW S1-S2 turn-on overlap time control mode

			S1-S2 ON
TRSW Control Mode	TR1	TR0	overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.8.

7. Pin Configuration

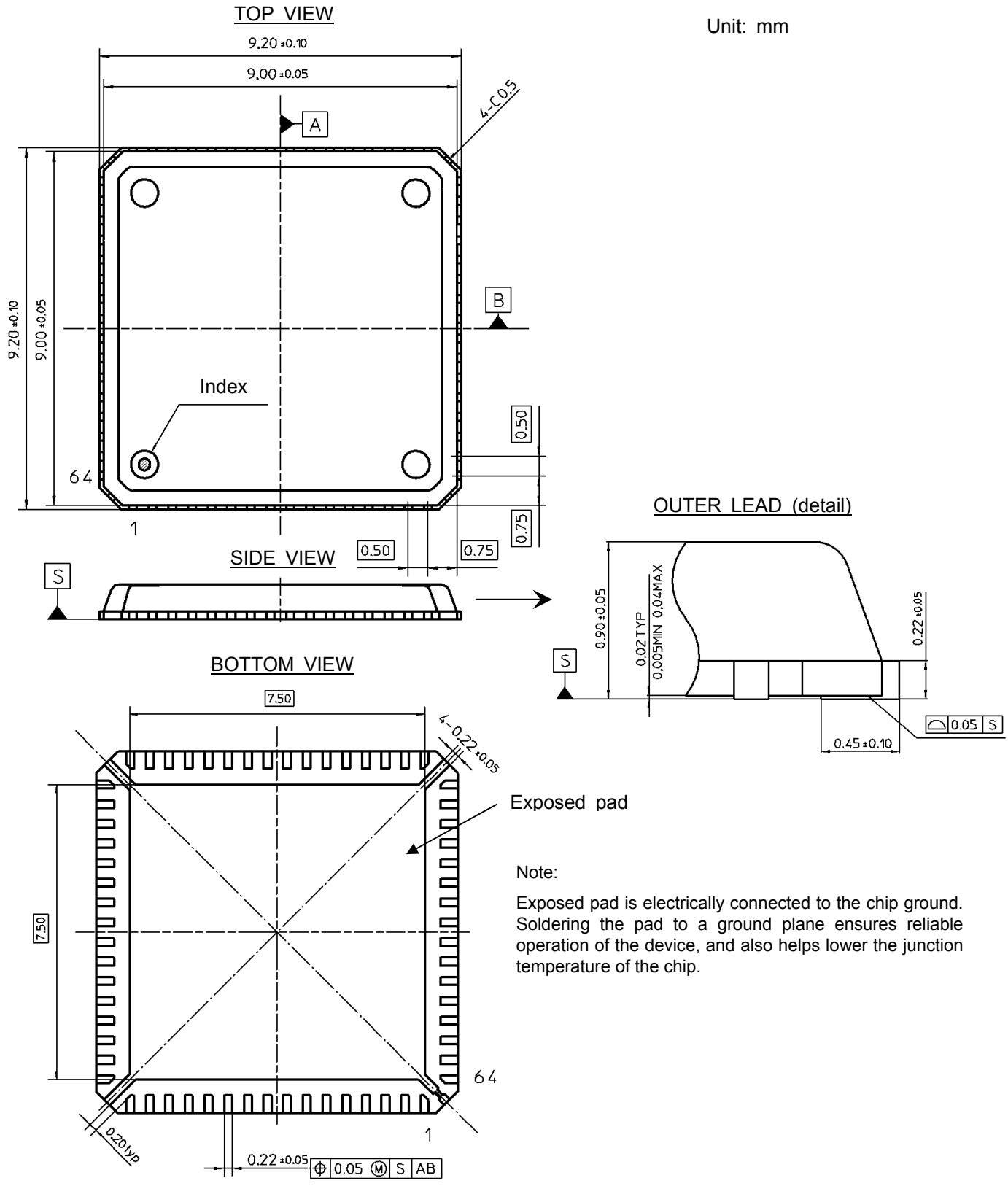
Table 16 Pin Configuration

Pin#	Pin Name	I/O	Function
1	$P_{IN}2$	I	Logic input of channel 2
2	$N_{IN}2$	I	Logic input of channel 2
3	$P_{IN}3$	I	Logic input of channel 3
4	$N_{IN}3$	I	Logic input of channel 3
5	$P_{IN}4$	I	Logic input of channel 4
6	$N_{IN}4$	I	Logic input of channel 4
7	V_{DD}	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	$P_{IN}5$	I	Logic input of channel 5
12	$N_{IN}5$	I	Logic input of channel 5
13	$P_{IN}6$	I	Logic input of channel 6
14	$N_{IN}6$	I	Logic input of channel 6
15	$P_{IN}7$	I	Logic input of channel 7
16	$N_{IN}7$	I	Logic input of channel 7
17	$P_{IN}8$	I	Logic input of channel 8
18	$N_{IN}8$	I	Logic input of channel 8
19	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
20	$LV_{OUT}8$	O	Low voltage output of channel 8
21	GND	-	Drive power ground (0V)
22	$HV_{OUT}8$	O	High voltage output of channel 8
23	V_{PP}	-	Positive high voltage power supply (0 to +100V)
24	$HV_{OUT}7$	O	High voltage output of channel 7
25	V_{NN}	-	Negative high voltage power supply (0 to -100V)
26	V_{FN}	-	Built-in power supply for N-MOS (N1) gate drive
27	$LV_{OUT}7$	O	Low voltage output of channel 7
28	$LV_{OUT}6$	O	Low voltage output of channel 6
29	V_{FP}	-	Built-in power supply for P-MOS (P1) gate drive
30	V_{PP}	-	Positive high voltage power supply (0 to +100V)
31	$HV_{OUT}6$	O	High voltage output of channel 6
32	V_{NN}	-	Negative high voltage power supply (0 to -100V)

Table 16 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
33	$HV_{OUT}5$	O	High voltage output of channel 5
34	GND	-	Drive power ground (0V)
35	$LV_{OUT}5$	O	Low voltage output of channel 5
36	GND	-	Drive power ground (0V)
37	GND	-	Drive power ground (0V)
38	EN	I	Control of drive output enable, Hi=off, Low=on (50kΩ internal pull-up resistor)
39	V_{SS}	-	Negative low voltage power supply (-5V)
40	V_{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
43	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
44	CC0	I	Lower bit of control of P1/N1 drive current (50kΩ internal pull-up resistor)
45	CC1	I	Upper bit of control of P1/N1 drive current (50kΩ internal pull-up resistor)
46	$LV_{OUT}4$	O	Low voltage output of channel 4
47	GND	-	Drive power ground (0V)
48	$HV_{OUT}4$	O	High voltage output of channel 4
49	V_{NN}	-	Negative high voltage power supply (0 to -100V)
50	$HV_{OUT}3$	O	High voltage output of channel 3
51	V_{PP}	-	Positive high voltage power supply (0 to +100V)
52	V_{FP}	-	Built-in power supply for P-MOS (P1) gate drive
53	$LV_{OUT}3$	O	Low voltage output of channel 3
54	$LV_{OUT}2$	O	Low voltage output of channel 2
55	V_{FN}	-	Built-in power supply for N-MOS (N1) gate drive
56	V_{NN}	-	Negative high voltage power supply (0 to -100V)
57	$HV_{OUT}2$	O	High voltage output of channel 2
58	V_{PP}	-	Positive high voltage power supply (0 to +100V)
59	$HV_{OUT}1$	O	High voltage output of channel 1
60	GND	-	Drive power ground (0V)
61	$LV_{OUT}1$	O	Low voltage output of channel 1
62	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
63	$P_{IN}1$	I	Logic input of channel 1
64	$N_{IN}1$	I	Logic input of channel 1

8. Package Outline

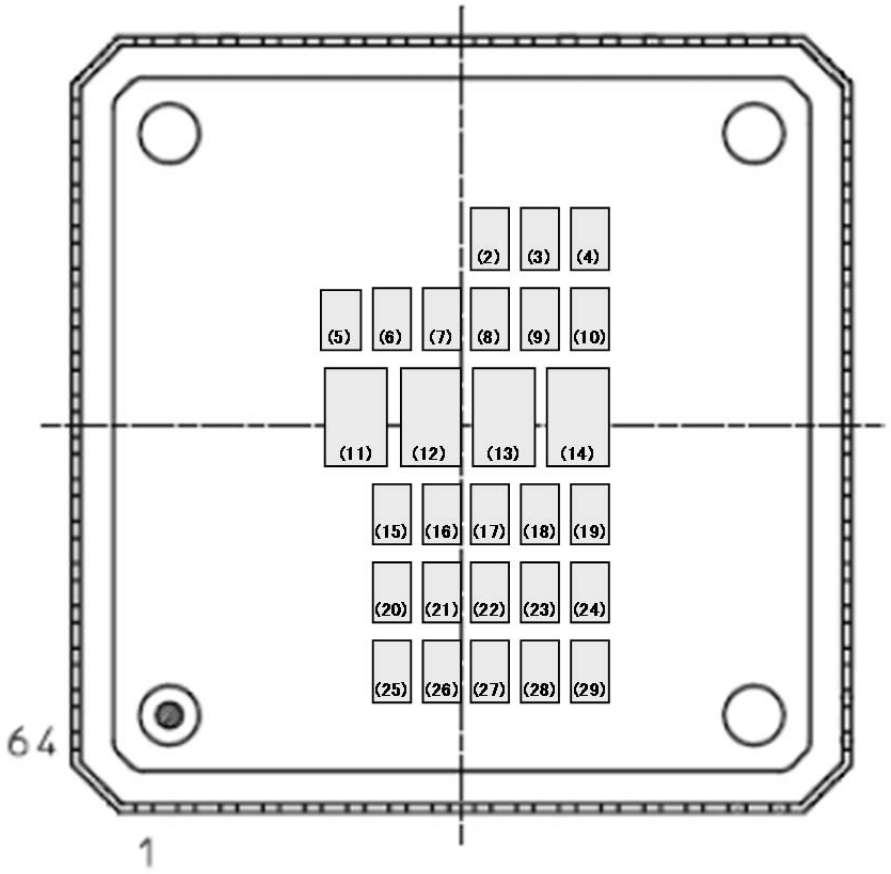


Note:

Exposed pad is electrically connected to the chip ground. Soldering the pad to a ground plane ensures reliable operation of the device, and also helps lower the junction temperature of the chip.

Fig.9 Package Outline (64-Lead QFN Package)

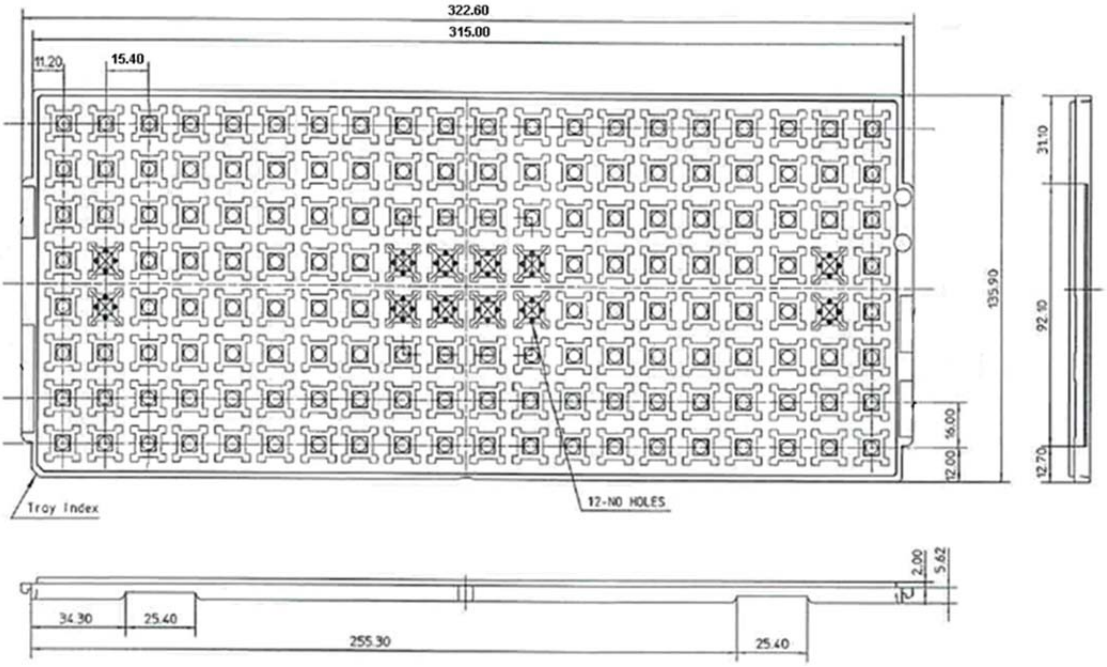
9. Package Marking



No.	Code
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc. " I ") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(14)	HDL6M05584 (product name)
(15)~(24)	Quality control code
(25)~(29)	Country of origin

Fig.10 Package Marking

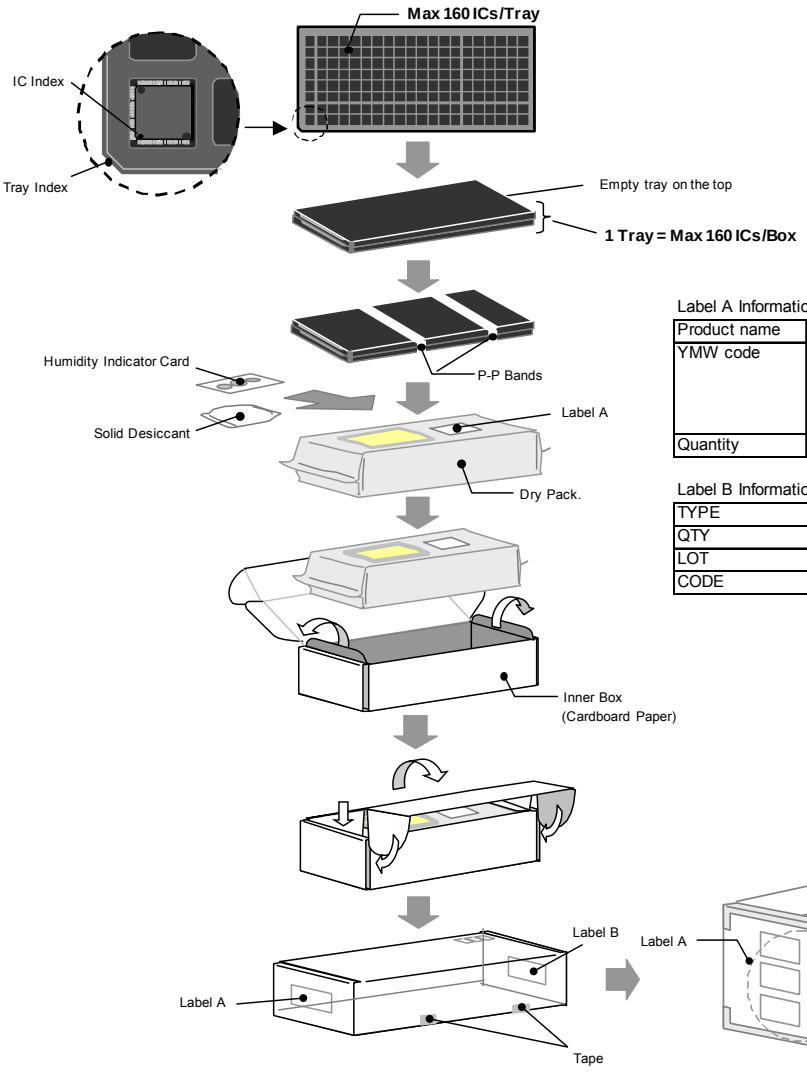
10. Transport Media, Quantity



Unit: mm

Fig.11 IC Tray Outline

1. Max 160 IC/Tray
2. 12 positions without holes (*)
3. PPE containing carbon and static proof
4. Heat proof: 130ºC, 24hr



Label A Information

Product name	HDL6M05584
YMW code	3 digits Y: Year sealed: The last one digit of the year M: Month sealed: A~M (exc. " I ") in the order of Jan. to Dec. W: Week sealed : 1~5
Quantity	Max 160 ICs/Box

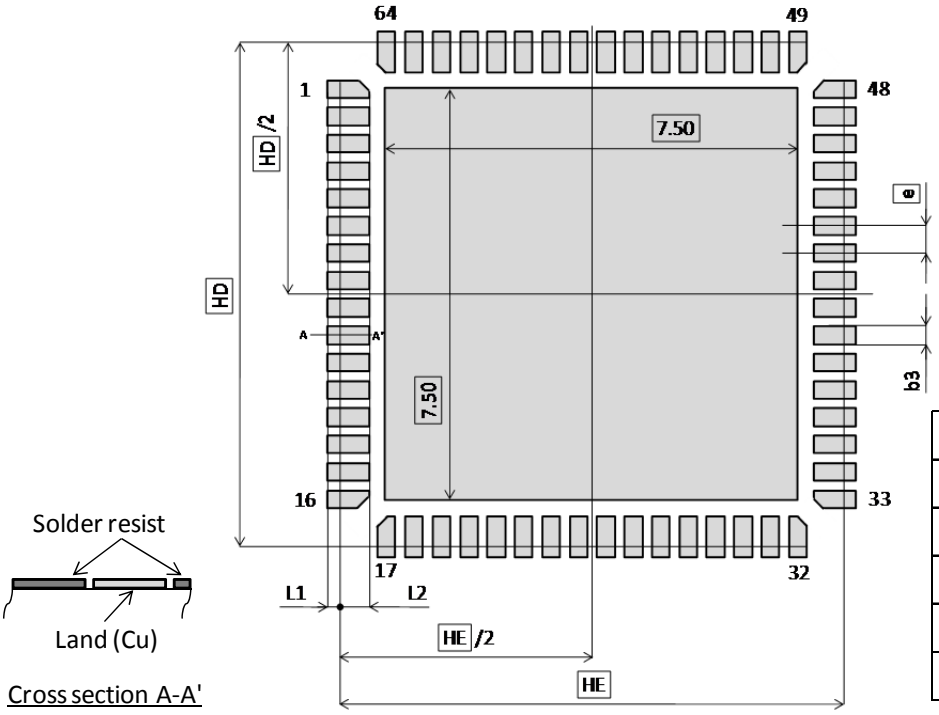
Label B Information

TYPE
QTY
LOT
CODE

Fig.12 Transport Media, Quantity

11. Mounting, Storage

11.1 Mounting Pad Design Example



Unit: mm

HD	9.20
HE	9.20
e	0.50
b3	0.32 ± 0.05
L2	0.55 ± 0.05
L1	0.20 ± 0.05

Fig.13 Mounting Pad Design Example

11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35 °C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 °C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable.
IR/Air reflow heating conditions are shown below.

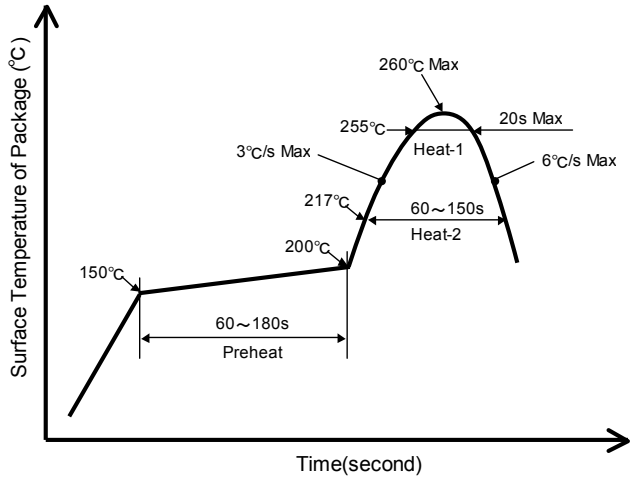


Fig.14 IR/Air Reflow Heating Conditions

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13.1.2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.

13.1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

13.1.4 Prevent friction with other materials made with high polymer.

13.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

13.1.6 Avoid dealing with or storing products in an extremely arid environment.

13.2 “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

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